WHAT IS CLAIMED IS:

1. A method of manufacturing a flash memory cell, comprising the steps of:

sequentially forming a tunnel oxide film, a first polysilicon layer and a pad nitride film on a semiconductor substrate;

forming a trench at the semiconductor substrate;

forming a trench insulating film by which the trench is buried and then performing a chemical mechanical polishing (CMP) process to isolate the trench insulating film;

removing the pad nitride film and then performing an etch process by which given portions of the trench insulating film are protruded;

depositing a second polysilicon layer on the entire structure and then patterning the second polysilicon layer to form a floating gate; and

forming a dielectric film and a control gate on the floating gate.

2. The method as claimed in Claim 1, further comprising the steps of:

before the tunnel oxide film is formed, forming a sacrificial oxide film on the semiconductor substrate;

performing a well ion implantation process and a threshold voltage ion implantation process for the semiconductor substrate, thus forming a well region and an impurity region; and

removing the sacrificial oxide film.

3. The method as claimed in Claim 2, wherein the sacrificial oxide film is formed in thickness of 70 through 100 Å by means of a dry or wet oxidization method at a temperature of 750 through 800 °C.

4. The method as claimed in Claim 1, wherein the tunnel oxide film is formed by performing a wet oxidization process at a temperature of 750 through 800 °C and then performing an annealing process using N_2 at a temperature of 900 through 910 °C for 20 through 30 minutes.

5. The method as claimed in Claim 1, wherein the first polysilicon layer is formed by a low-pressure chemical vapor deposition (LP-CVD) method having a temperature of 580 through 620 °C and low pressure of 0.1 through 3Torr under a SiH_4 or Si_2H_6 and PH_3 gas atmosphere.

6. The method as claimed in Claim 1, further comprising the step of after the trench is formed, performing an annealing process using hydrogen to make the corner of the trench rounded.

7. The method as claimed in Claim 6, wherein the annealing process is performed using an RTP or FTP equipment at a temperature of 600 through 1050℃ for 5 through 10 minutes.

8. The method as claimed in Claim 6, wherein the flow rate of hydrogen is 100 through 2000sccm.

9. The method as claimed in Claim 1, further comprising the step of after the trench is formed, forming a liner nitride film on the entire structure.

10. The method as claimed in Claim 9, wherein the liner nitride film is formed in thickness of 100 through 500 Å by a LP-CVD method at a temperature of 650 through 770 °C and low pressure of 0.1 through 1Torr.

11. The method as claimed in Claim 1, further comprising the step of after the trench is formed, performing a pre-treatment cleaning process in order to etch the tunnel oxide film by a desired thickness.

12. The method as claimed in Claim 11, wherein the pre-treatment cleaning process is performed using DHF and SC-1 or BOE and SC-1.

13. The method as claimed in Claim 1, wherein the trench insulating film is formed in thickness of 4000 through 10000 Å using a gap filling method.

14. The method as claimed in Claim 1, wherein the CMP process is performed to remain the pad nitride film by a given thickness.

15. The method as claimed in Claim 1, wherein the etch process is a cleaning process using H_3PO_4 dip out.

16. The method as claimed in Claim 1, wherein an upper portion of the second polysilicon layer has a concavo-convex shape by the trench insulating film.

17. The method as claimed in Claim 16, wherein the second polysilicon layer is formed in thickness of 400 through 1000 Å.

18. The method as claimed in Claim 1, wherein the floating gate includes the first and second polysilicon layers.

19. The method as claimed in Claim 1, wherein the dielectric film comprises:

a first oxide film that is formed in thickness of 35 through 60 Å by using HTO using DCS(SiH_2Cl_2) and N_2O gas as a source;

a nitride film that is formed in thickness of 50 through 65 Å on the first oxide film by means of a LP-CVD method using NH_3 and DCS gas as a reaction gas at a temperature of 650 through 800 °C and low pressure of1 through 3Torr; and

a second oxide film that is formed in thickness of 35 through 60 Å on the nitride film by using HTO using DCS(SiH_2Cl_2) and N_2O gas as a source.

20. The method as claimed in Claim 1, wherein the control gate is formed to have a dual structure of a doped layer and an undoped layer by means of a LP-CVD method.

21. The method as claimed in Claim 20, wherein the ratio in the thickness of the doped layer and the undoped layer is 1:2 through 6:1, and the entire thickness of the doped layer and the undoped layer is 500 through 1000 Å.

22. The method as claimed in Claim 1, wherein the control gate is formed at a temperature of 510 through 550 °C and low pressure of 0.1 through 3Torr.

23. The method as claimed in Claim 1, further comprising the step of after the control gate is formed, forming a tungsten silicide layer using reaction of $MS(SiH_4)$ or DCS and WF_6 at a temperature of 300 through 500 °C at the stoichiometry of 2.0 through 2.8. .